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Characterization of the Calocube front-end electronics coupled with VTH2090 photodiode(*)

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Abstract

The calorimeter Calocube is designed to bring a significant contribution to the direct observation of cosmic rays at high energy. This calorimeter will consist of scintillator (CsI(Tl)) cubes read out by photodiodes. In this report we present a study of the response of the front-end electronics of the Calocube prototype, that consists of 9 CASIS chips, coupled with the VTH2090 photodiode. The CASIS chip is a double-gain, large dynamic range Front-end ASIC for silicon detectors Read-Out. Thanks to some PSpice simulation, confirmed by measurements on the real circuit, we understood the causes of some anomalous behaviors of the front-end electronics that could disrupt the proper functioning of the prototype. We present also a few different circuit configurations that could partially eliminate this effects.

1 Introduction

Calocube [1] is a homogeneous calorimeter instrumented with Cesium iodide (CsI) crystals, whose geometry is cubic and isotropic, so as to detect particles arriving from every direction in space, thus maximizing the acceptance. The granularity is obtained by filling the cubic volume with small cubic CsI crystals. To cover the huge required dynamic range (from 1 MIP for non interacting protons, useful for calibration purposes, up to 10^7 MIPs in one single crystal for 1 PeV interacting hadrons) the photosensors and the readout electronics must be carefully chosen and designed.
Prototype construction and testing activities have been carried out in parallel to simulation studies. A matrix of 126 CsI(Tl) crystals (14 layers, 3×3 crystals per layer) has been assembled in a modular mechanical structure. Each crystal was coupled with a large area Excelitas VTH2090 photodiode which ensures a linear response in the range from 0.3 to 104 MIP, and 9 CASIS chips have been used for the readout.

The CASIS chip [2] has been specifically developed by INFN section of Trieste for calorimetric space applications. Every chip consists of 16 independent channels, with a charge sensitive amplifier, a correlated double sampling system and automatic gain selection. Automatic gain selection switches between two gain values depending on the injected charge. The small power consumption of a single channel ($2.8\,mW$) associated with the low noise ($3000\,e^-$ for $100\,pF$ input capacitance) and the large maximum input charge ($53\,pC$) are perfectly suited for the Calocube design.

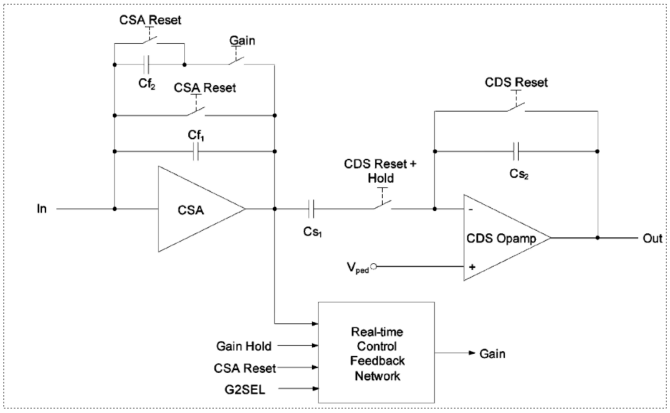

Figure 1: Schematic block diagrams of one processing channel of the CASIS chip.

Fig. 1 represents the schematic block diagram of the front-end section. It contains a charge sensitive amplifier (CSA) followed by a correlated double sampling filter (CDS). To realize the required dynamic rage, a new architecture of the CSA feedback has been implemented. It consists of a double-gain loop with a real-time select circuitry: a $1.6\,pF$ capacitor is permanently connected to a folded cascode amplifier, to set the high gain, while a second large capacitor ($30.4\,pF$) is automatically inserted in parallel when the input signal exceeds a given threshold. A switch is used to reset periodically the pre-amplifier. The CSA output is sampled by a CDS filter: when a trigger is present, the Hold signal (this is the signal that enables the ADC to sample) is generated after a fixed (adjustable) delay from the last Reset pulse, and at the output of the CDS operational amplifier appears the difference between the baseline and the signal. The DC pedestal of the CDS output (normally set at $900\,mV$) can be adjusted externally by means of the V_{ped} bias. A Gain-Hold signal is used to avoid possible noise-induced gain changes shortly before the Hold time when the input charge is close to the threshold.

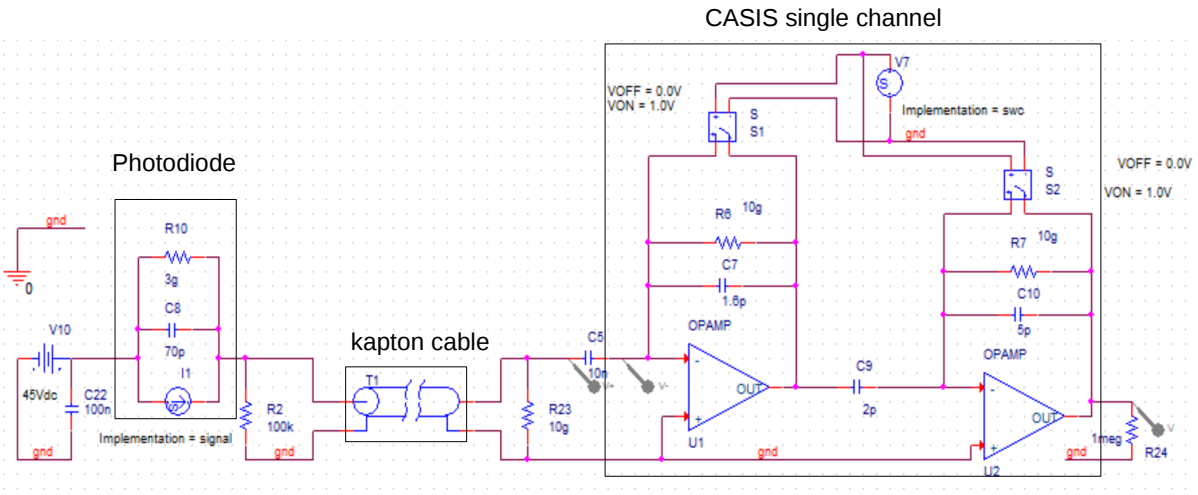

Figure 2: Schematic of the Orcad project: the first part of the circuit is the equivalent circuit of the photodiodes, the kapton cable is modelled as a lossless transmission lines and the last part of the circuit is a simple model of a single CASIS channel.

The Excelitas VTH2090 photodiode consists of a chip with an area $9.2 \times 9.2\ mm^2$ mounted in a black ceramic package. This device has a $10\ nA$ dark current and junction capacitance $70\ pF$ at $30\ V$ reverse bias voltage. The peak of the spectral response is $65\ A/W$ for $\lambda = 960nm$.
The photodiodes are connected to the front-end electronics by kapton cables and $10\ nF$ coupling capacitors.

2 OrCAD project and PSpice simulations

To study the response of the CASIS chips with AC coupled photodiode we have developed a PSpice project using OrCAD Capture software. Fig. 2 presents the simulated circuit. Starting from the left of the figure, the first part is the equivalent circuit of the photodiodes reverse bias ($V_R = 45\ V$). The VTH2090 photodiode is modelled as a current generator with $70\ pF$ parallel capacitor (C8) and $3\ G\Omega$ parallel resistor (R10). The value of R10 is calculated according to the dark current given in the Excelitas datasheet: $R10 = 10nA/30V$. The kapton cable is modelled as a lossless transmission lines with characteristic impedance $Z_0 = 50\Omega$. The last part of the circuit is a simple model of a single CASIS channel, that consists in two ideal op-amp: the first one is used to simulate the CSA with only the small feedback capacitor, while the second simulates the CDS. In this project we have studied the high gain mode only. The exact values of C9 and C10 are unknown so we have chosen two capacitances that correctly reproduce the response of the real circuit (as explained below). Thanks to the switches S1 and S2 we could simulate the periodic Reset that discharge the feedback capacitors C7 and C10 but we have not implemented the Hold-switch present in fig. 1. As explained below, this choice does not compromised the final result.

2.1 Simulation parameters and results

In the first simulation we have observed the output voltage and the differential voltage signal on the coupling capacitor C5 measured as a function of time. For this purpose we have used PSpice Time Domain simulation and the input stimulus (I1) was a current pulse with the following parameters:

I_{min}	I_{max}	Width	Rise Time	Fall time
$0\mu A$	$100nA$	$4\mu s$	$10ns$	$50ns$

The input stimulus has been chosen to match the LED light that has been used in the measurement described in §2.2. The period of the Reset is $20\ \mu s$, equal to the default value that has been used during the beam tests performed on the Calocube prototype, and the simulation run time is $100\ \mu s$. The result is presented in fig. 3: the red line is the differential C5 signal multiplied by 1000, because it was too small to be displayed (maximum amplitude $\sim 40\ \mu V$) and the green line is the output voltage of the single channel (measured by $1\ M\Omega$ resistor). The C5 signal rise time is equal to the pulse width of the input stimulus, but the fall time is very long: this could be due to the capacitor discharging through the R2 resistor ($100\ k\Omega$) with a RC time constant equal to $\sim 1\ ms$. To test this hypothesis we have repeated the simulation with a run time equals to $5000\ \mu s$ and the period of the Reset amounting to $200\ \mu s$. The result is presented in fig 4 and it confirms that the time constant is about $1\ ms$. The

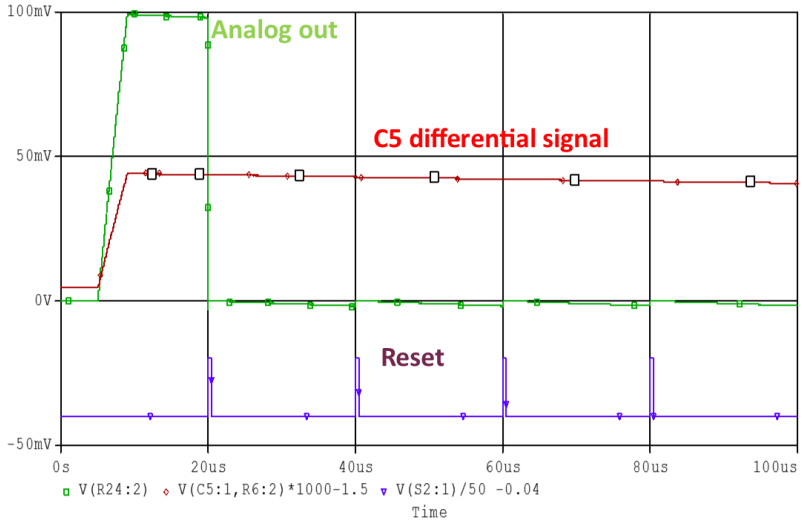

Figure 3: First simulation result (Reset period 20 μs, total time 100 μs): output voltage (green line) and differential C5 signal multiplied by 1000 (red line) as a function of time.

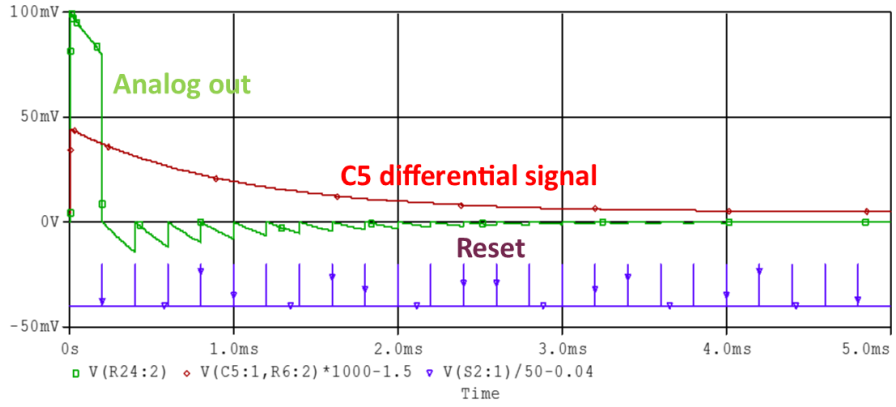

Figure 4: Second simulation result (Reset period 200 μs, total time 5000μs): output voltage (green line) and differential C5 signal multiplied by 1000 (red line) as a function of time.

output signal has the same rise and fall time of C5 but during each Reset the voltage goes back to zero.
These simulations clearly show two anomalous behaviors of the front-end electronics:

1. the signal of C5 capacitor discharges through the resistor and absorbs a part of the charge from integrator capacitor C7 so the output signal is not stable during the integration (the total integration time is equal to the time interval between Reset and Hold)

2. after the first Reset the output signal is not stable for a very long time ($\sim$ 1 ms) so there will be a overlap between high rate signals.

The first effect could disrupt the energy resolution of the prototype: due to the fact that the cosmic rays are random the Trigger and the Hold signal is not fixed so the entity of capacitor discharging in presence of scintillation signal is unknown. The second effect translate in a limiting rate of the acquisition with a dead time of approximately $\sim$ 1 ms. If a small signal arrives immediately after a large one it can be completely hidden by the capacitor discharging.

2.2 Response of the real circuit

We have performed some measurements of the output signal of the real circuit to test the simulation accuracy. We have used a single photodiode illuminated directly by a green LED and coupled to CASIS chip with a kapton cable. The LED source was a voltage pulse and the pulse parameters have been chosen to match the CsI(Tl) response:

V_{min}	V_{max}	Width	Period	
$0V$	$4V$	$4\mu s$	$10ns$	$\sim 50ms$

The response of the VTH2090 is very fast, about $1 - 10ns$, and also the rise and fall time are very short. During this measurements the period of the Reset has been setted to $200\ \mu s$. Analog output of the CASIS has been sampled with LeCroy Oscilloscope and the result is shown in fig 5.

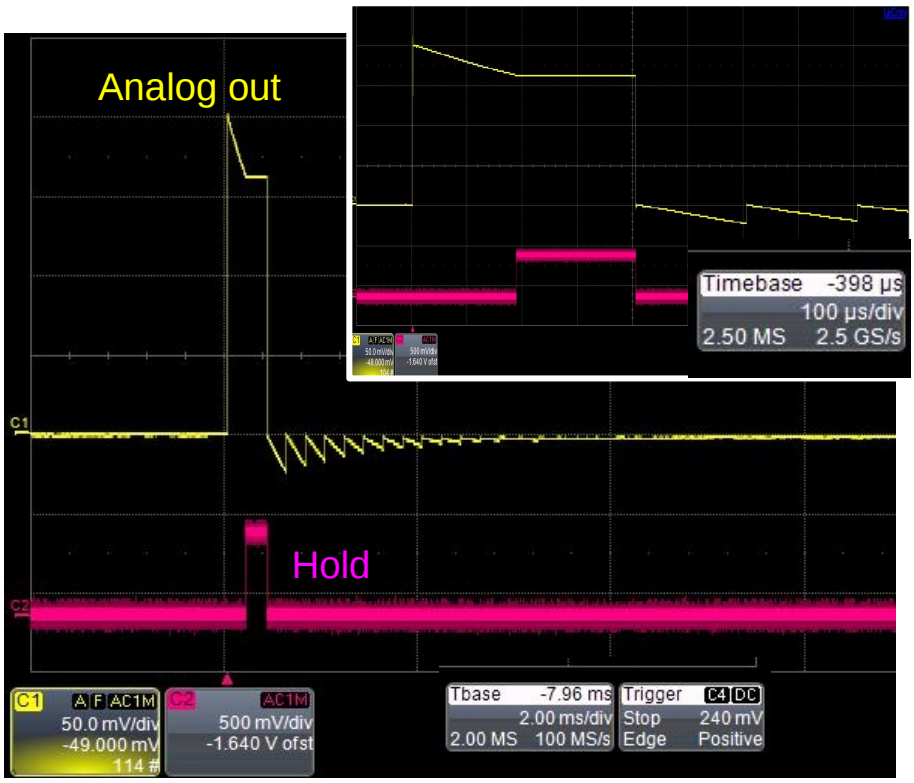

Figure 5: Analog output of the CASIS chip (Reset period 200 μs): the output voltage is the yellow line and the Hold signal is the red line. In the top-right is shown an enlargement of the picture.

As one can see that the measured analog output parameters, both the signal shape and the time constant, correspond to the simulation results. The only difference in the signal shape is present when the Hold is high, as we expect. However the only effect of the Hold signal is to freeze the output for a fixed time interval. The signal amplitude is different because the values of C9 and C10 are still unknown. Furthermore it is very difficult to understand the exact value of the photocurrent produced from the photodiode.

3 Different front-end electronics configuration

New simulation and measurements have been performed to find the solution. The $10\ nF$ coupling capacitor C5 has been replaced by $100\ nF$: both the simulation and the measurements result, in this conditions, are shown in fig. 6.
The capacitor discharge is slower that the previous measurements so the analog output has a slower decrease than before. The detector resolution, in this case, is better but we have to wait a long time to have a stable output after the signal, equal to $\sim 100nF \cdot 100k\Omega = 10ms$.
We have repeated the same test with $C5 = 10\ nF$ and $R2 = 1000\ k\Omega$ and we found a very similar result compared with the previous, as we expected.
In summary the replacement of C5 and/or R2 will improve the circuit performance with respect to one of the two effects explained above (§2.1) but will worsen the other. In order to improve the energy resolution of the calorimeter a big capacitor (and/or a big resistor) is required so that the signal fall time is very long: for high rate particles (like low energy proton out of the atmosphere) there is not enough time for the capacitor discharge and so this component has to store an increasing number of electrostatic charges. This could be a problem for a long time cosmic rays exposure of the device.

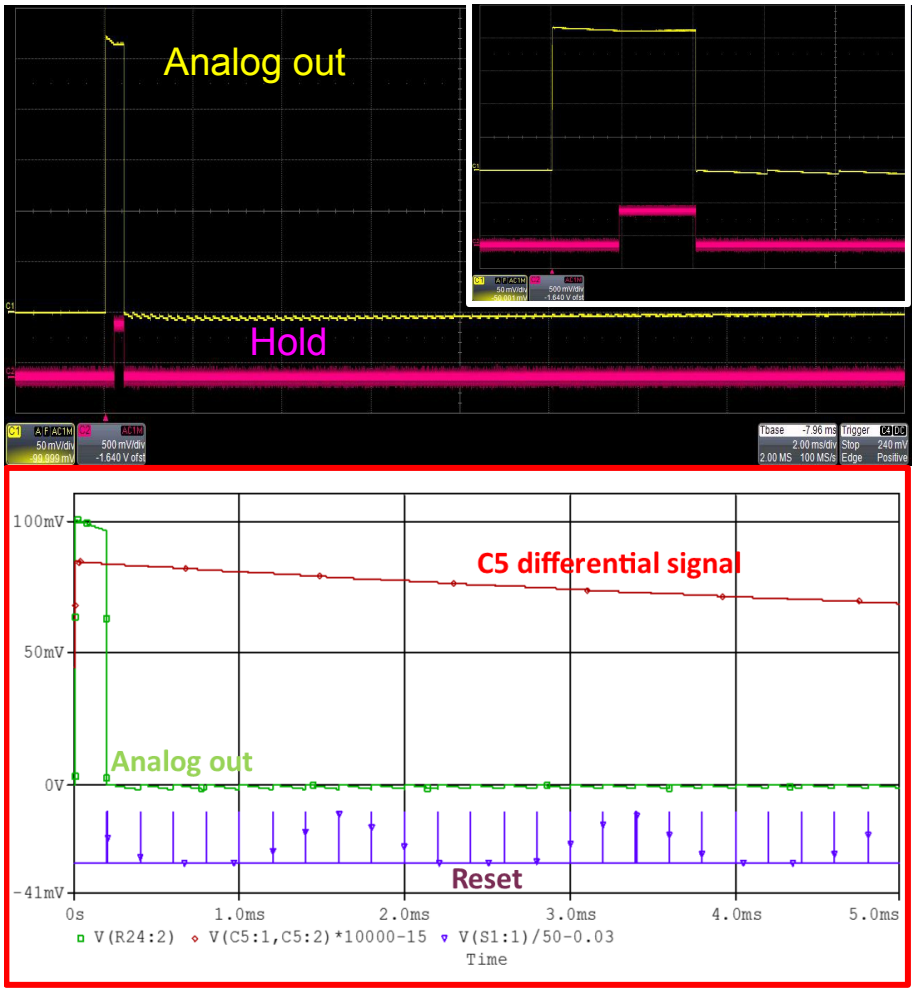

Figure 6: Top: the analog output of the CASIS chip for $C5 = 100nF$ and $R2 = 100k\Omega$. In the top-right is shown an enlargement of the picture. Bottom: simulation result, output voltage (green line) and differential C5 signal multiplied by 10000 (red line) as a function of time.

We have simulated DC coupled circuit with the scope to find the solution of this problems. The simulation result is shown in fig. 7
The output, without the input stimulus, grows as a linear function of time, due to the integration of the photoiode dark current. When a stimulus is present the output voltage become the sum of both dark current and stimulus integral. If the dark current is stable in time, thanks to the subtraction pedestal we can isolate the signal from the dark current (the integral windows is fixed). In real application the dark current depend on the temperature and other environmental factors so it will be necessary to run some tests on the real circuit.

In order to implement the DC coupling scheme we need to know the features of the chip input. We have tried to measure the CASIS input bias voltage, that should be close to zero, as we have supposed during the simulations. Tektronix P6205 FET probe has been used to minimize the instrument impact to the measured system. This expedient is, unfortunately, not enough to achieve a good measurement: when the probe is connected to the chip the output has an anomalous response. The signals acquired during one of these measurements is shown in figure 8: the blue line is the output signal, the yellow line is the input voltage and the green line is the trigger. As one can see the output signal is completely different respect to the previous measurement.

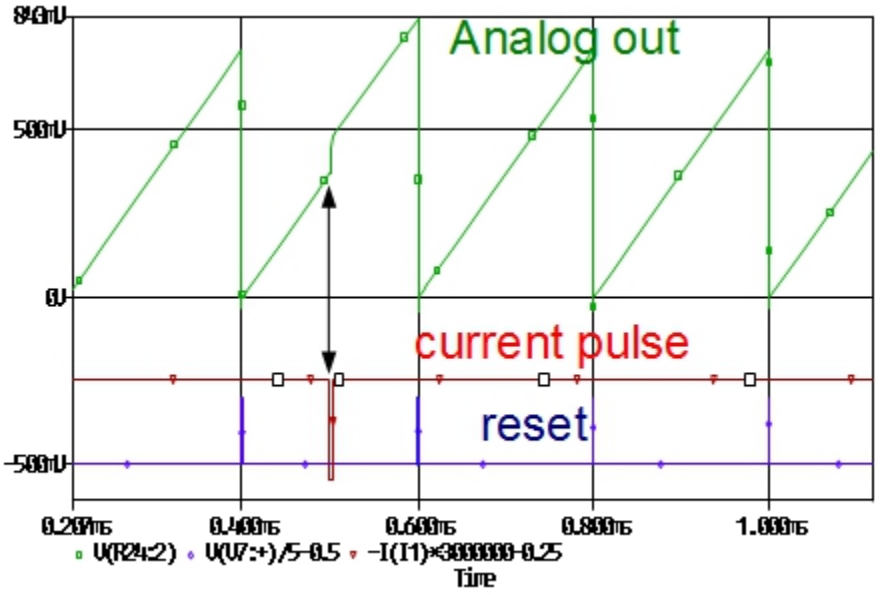

Figure 7: DC coupling simulation result, output voltage (green line) current stimulus multiplied by $3 \cdot 10^6$ (red line) and reset signal (violet line) as a function of time.

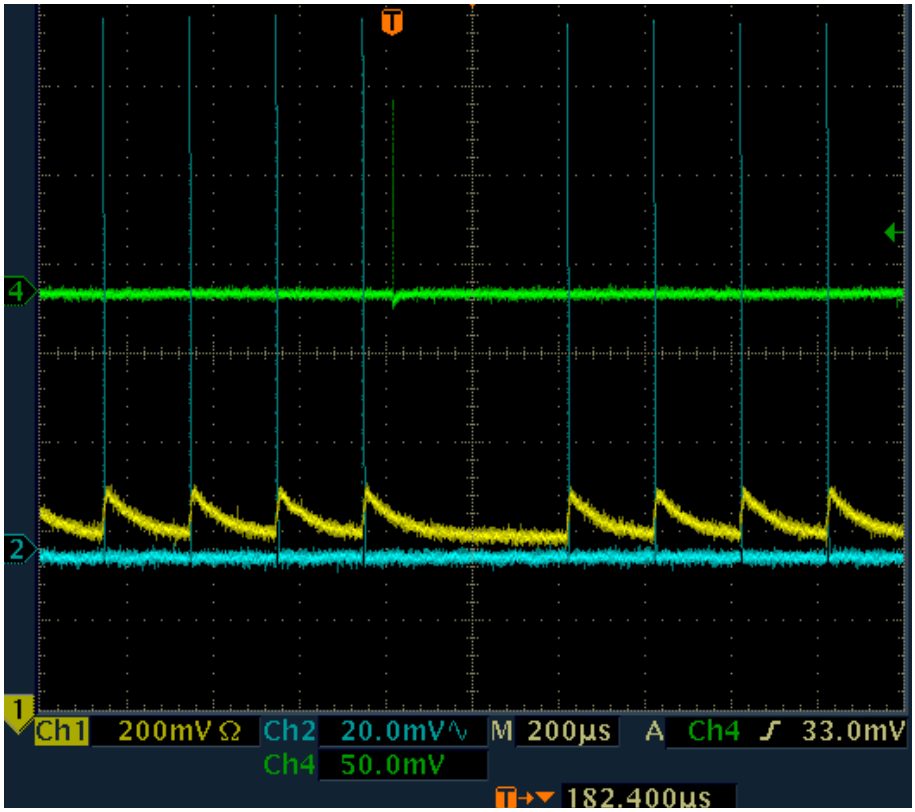

Figure 8: Input and output signal measured with a FET probe: the blue line is the output signal, the yellow line is the input voltage and the green line is the trigger.

4 Conclusions

In this report we have studied the response of a single channel of the CASIS chips AC coupled with the VTH2090 photodiode. Thanks to the PSpice project used to simulate the CASIS+photodiode, in parallel to measurements on the real circuit, we have found two different anomalous behaviors of the Calocube front-end electronics:

1. the output signal is not stable during the integration and so the calorimeter resolution will be disrupted
2. If we want to remove any overlap we have to wait a long time between the signal.

In order to find a solution we have tried a different configuration of this circuit. We have replaced the coupling capacitor (and/or the protection resistor) with a bigger one: the detector resolution is better but we have longer dead time after the signal. We have simulated also a possible DC coupling because of this result. In this configuration the two effects disappear but we have to take care of the photodiode dark current integral.
We could not implement the DC coupling in the real circuit because of the difficulty to provide a characterization of chip input.
In the future we could repeat the measure of the input bias voltage using an operational amplifier with low bias current (i.e. the AD549, maximum bias current $\sim 60\ fA$) instead of the FET-probe.

In conclusion: we have found the anomalous behaviors of the Calocube front-end electronics which seems to be caused bay coupling between the photodiode and the chip that is not very congruent.

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